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EXAMINER	
WOOD, WILLIAM H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/435,070	SINHAROY, BALARAM	
	Examiner	Art Unit	
	William H. Wood	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 08 September 2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 10 and 21-40 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 10 and 21-40 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 10 and 21-40 have been examined.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al., "Alternative Implementations of Hybrid Branch Predictors" in view of Talcott et al. (USPN 6,289,441) and in further view of Shimomura et al. (USPN 5,737,381).

In regard to claim 10, Patt disclosed the limitations:

- *A processing system comprising:*
  - *a first branch history table comprising a plurality of bimodally accessed entries for storing a first set of branch prediction bits* (page 253; item 2 under section 3.1)*;*
  - *a second branch history table comprising a plurality of entries for storing a second set of branch prediction bits* (page 253, item 4, under section 3.1)*;*
  - *a selector for selecting in response to a selection control bit selected from a set of selection control bits, a bit from a selected one of said sets of bits*

accessed from said first and second branch history tables (page 255, section 4, 4.1 and Figure 2)*; and*

- *a selector table comprising a plurality of entries for storing said a set of selector bits as a function of a performance history of said first and second sets of branch prediction bits stored in said first and second branch history tables, wherein said each said entry in said tables comprises a 1-bit counter* (page 252, section 2; page 255, section 4, 4.1 and Figure 2; a 2-bit counter would naturally "comprise" a 1-bit counter).

Patt did not explicitly state *fetch-based branch history table*. **Talcott** demonstrated that it was known at the time of invention to construct fetch-based branch history tables wherein a table produces a prediction value for multiple branches within a fetch group (column 3, line 58 to column 4, line 25). It would have been obvious to one of ordinary skill in the art at the time of invention to implement **Patt**'s branch prediction scheme with fetch groups as found in **Talcott**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs.

Neither **Patt** nor **Talcott** explicitly stated entries comprising a 1-bit counter. **Shimomura** demonstrated that it was known at the time of invention to implement 1-bit counters (Figures 1-5 and 7-9). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the counters of **Patt** and **Talcott** as 1-bit

counters as taught by **Shimomura**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to implement a simple design structure for easy understanding or implement less hardware to save space and thus money (**Talcott**: column 4, lines 15-19, implementing a counter for each instruction would imply a need to save space and cost, by using less hardware).

In regard to claim 30, Patt and Talcott did not explicitly state the limitation *wherein said each said entry in said tables comprises a 1-bit counter.* Shimomura demonstrated that it was known at the time of invention to implement 1-bit counters (Figures 1-5 and 7-9). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the counters of Patt and Talcott as 1-bit counters as taught by Shimomura's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to implement a simple design structure for easy understanding or implement less hardware to save space and thus money (Talcott: column 4, lines 15-19, implementing a counter for each instruction would imply a need to save space and cost, by using less hardware).

3. Claims 21-29 and 31-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al., "Alternative Implementations of Hybrid Branch Predictors" in view of Talcott et al. (USPN 6,289,441).

In regard to claim 21, **Patt** disclosed the limitations:

- *Branch prediction circuitry comprising:*
  - *a bimodal branch history table comprising a plurality of entries each for storing a prediction value and accessed by selected bits of a branch address* (page 253, item 2 under section 3.1)*;*
  - *a branch history table comprising a plurality of entries for storing a prediction value and accessed by a pointer generated from selected bits of said branch address and bits from a history register* (page 253, item 4 under section 3.1)*; and*
  - *a selector table comprising a plurality of entries each for storing plurality of selection bits and accessed by a pointer generated from selected bits from said branch address and bits from said history register* (page 255, section 4, first paragraph and section 4.1, last paragraph; page 255, right column , second paragraph, demonstrates pointer being generated; Figure 2)*, each said selector bit used for selecting between a bimodal prediction value accessed from the bimodal history table and a prediction value accessed from said fetch-based history table* (page 252, section 2; page 255, section 4.1, first paragraph; page 252, section 2; each bit enables the selection of the single predictor in that it is part of the counter).

Patt did not explicitly state *fetch-based branch history table* with each entry *operable for containing bits representing a prediction value for a plurality of branches in a fetch group.* **Talcott** demonstrated that it was known at the time of invention to construct fetch-based branch history tables wherein a table produces a prediction value for

multiple branches within a fetch group (column 3, line 58 to column 4, line 25; column 4, lines 15-18). It would have been obvious to one of ordinary skill in the art at the time of invention to implement **Patt**'s branch prediction scheme with fetch groups as found in **Talcott**'s teaching and thus produce a table with entries which represent predictions for each instruction in a group. This implementation would have been obvious because one of ordinary skill in the art would be motivated to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs (column 1, lines 54-67).

In regard to claim 22, Patt and Talcott did not explicitly state the limitations:

- *circuitry for updating said bimodal and fetch-based branch history tables operable to:*
  - *set a corresponding entry in each of said bimodal and fetch-based branch history tables to a first value when a branch is taken at branch resolution time; and*
  - *set a corresponding entry in each of said bimodal and fetch-based branch history tables to a second value when a branch is not taken at branch resolution time.*

Patt demonstrated that it was known at the time of invention to utilize the most accurate branch prediction (page 255, section 4 and section 4.1, right column, top two paragraphs). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Patt and Talcott's hybrid branch prediction as updating entries in

each of the bimodal and fetch-based tables with one or another value based upon the accuracy of prediction as suggested by Patt's own teachings. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide an accurate history as to which type of single predictor is correct in order to be more successful in future predictions.

In regard to claim 24, Patt and Talcott further disclosed the limitations:

- *circuitry for updating said selector table operable to:*
- *update a corresponding bit in a selected entry in said selector table with a first value when a bimodal prediction value from said bimodal branch history table correctly represents a corresponding branch resolution* (Patt: page 252, section 2, first paragraph)*; and*
- *update a corresponding bit in a selected entry in said selector table with a second value when a fetch-based prediction-value from said fetch-based branch history table correctly represents the corresponding branch resolution* (Patt: page 252, section 2, first paragraph).

In regard to claim 25, Patt and Talcott further disclosed the limitation *wherein the plurality of selection bits are operable for selecting a first subset of prediction values from the bimodal branch history table and a second subset of prediction values from the fetch-based branch history table* (Patt: page 252, section 2; clearly the selector selects one branch predictor when it is useful and the other when it is useful).

In regard to claim 28, Patt disclosed the limitations:

- *A processing system comprising:*
  - *a first branch history table comprising a plurality of bimodally accessed entries, each entry for storing a first set of branch prediction bits* (page 253; item 2 under section 3.1)*;*
  - *a second branch history table comprising a plurality of entries each entry for storing a second set of branch prediction bits* (page 253, item 4, under section 3.1)*;*
  - *a selector for selecting, in response to a plurality of selection control bits, a set of prediction bits from a selected one of said sets of bits accessed from said first and second branch history tables* (page 255, section 4, 4.1 and Figure 2)*; and*
  - *a selector table comprising a plurality of entries, each entry for storing a plurality of selection control bits wherein the selection control bits are set as a function of a performance history of corresponding first and second sets of branch prediction bits stored in said first and second branch history tables* (page 255, section 4, 4.1 and Figure 2; page 252, section 2; each bit enables the selection of the single predictor in that it is part of the counter)

Patt did not explicitly state *fetch-based branch history table.* **Talcott** demonstrated that it was known at the time of invention to construct fetch-based branch history tables

wherein a table produces a prediction value for multiple branches within a fetch group (column 3, line 58 to column 4, line 25). It would have been obvious to one of ordinary skill in the art at the time of invention to implement **Patt**'s branch prediction scheme with fetch groups as found in **Talcott**'s teaching and thus produce a table with entries which represent predictions for each instruction in a group. This implementation would have been obvious because one of ordinary skill in the art would be motivated to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs (column 1, lines 54-67).

In regard to claim 29, Patt and Giacalone did not explicitly state the limitation *wherein said entries of said selector table are accessed using fetch-based accessing*. Talcott demonstrated that it was known at the time of invention to construct fetch-based branch history tables wherein an entry represents a prediction value for multiple branches within a fetch group (column 3, line 58 to column 4, line 25). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Patt's single predictor selector mechanism with fetch groups as found in Talcott's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to increase branch prediction accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs (Talcott: column 1, lines 54-67). Additionally, the two level single predictor and the two level hybrid predictor mechanism function much the same, further leading one to adapt what is adapted for one to the other (in this case fetch-based accessing).

In regard to claim 31, Patt and Talcott did not explicitly state the limitation *wherein said first and second branch history tables and said selector table form a portion of a branch execution unit* (Talcott: Figure 1, element 100).

In regard to claim 32, Patt and Talcott further disclosed the limitation *wherein said branch execution unit forms a part of a microprocessor* (Patt: Abstract indicates superscalar processors).

In regard to claim 33, Patt and Talcott did not explicitly state the limitation *further comprising memory coupled to said microprocessor.* Offical Notice is taken that it was known at the time of invention to couple memory to a microprocessor. It would have been obvious to one of ordinary skill in the art at the time of invention to implement the processor of Patt and Giacalone with memory couple to it. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide a store of data and instructions for which a processor can operate, in excess of the comparatively small amount of data and instructions stored directly within the processor.

In regard to claim 34, **Patt** disclosed the limitations:

- *A method of performing branch predictions in a processing system including a bimodal branch history table, a branch history table and a selector table, the method comprising the substeps of:*
  - *accessing the bimodal branch history table to retrieve a first set of branch prediction bits* (page 253, item 2 under section 3.1)*;*
  - *accessing the branch history table to retrieve a set of second branch prediction bits* (page 253, item 4 under section 3.1)*;*
  - *selecting between the first and second sets of branch prediction bits in response to corresponding bits retrieved from the selector table* (page 255, section 4, 4.1 and Figure 2; page 252, section 2)*; and*
  - *updating the selector table as a function of actual branch resolution* (Patt: page 252, section 2, first paragraph)

Patt did not explicitly state *fetch-based branch history table* with each entry *operable for containing bits representing a prediction value for a plurality of branches in a fetch group*. **Talcott** demonstrated that it was known at the time of invention to construct fetch-based branch history tables wherein a table produces a prediction value for multiple branches within a fetch group (column 3, line 58 to column 4, line 25; column 4, lines 15-18). It would have been obvious to one of ordinary skill in the art at the time of invention to implement **Patt**'s branch prediction scheme with fetch groups as found in **Talcott**'s teaching and thus produce a table with entries which represent predictions for each instruction in a group. This implementation would have been obvious because one of ordinary skill in the art would be motivated to increase branch prediction

accuracy for many instructions, which is increasingly necessary for superscalar pipeline designs (column 1, lines 54-67).

Patt and **Talcott** did not explicitly state *wherein a sum of a number of bits in the first set of branch prediction bits and a number of bits in the second set of branch prediction bits is not less than a number of instructions in a fetch group*. **Talcott** demonstrated that it was known at the time of invention to construct fetch groups (column 3, line 58 to column 4, line 25). It would have been obvious to one of ordinary skill in the art at the time of invention that an implementation of the combination with **Talcott**, if one prediction bit came from the first table and one bit came from the second table it would not be less than the instructions in a fetch group if that group were composed of two instructions. This implementation of two instructions in a fetch group would have been obvious (over a larger number) because one of ordinary skill in the art would be motivated to develop systems of reduced instruction throughput to alleviate complexity. Furthermore, this implementation would have been obvious because one of ordinary skill in the art would recognize the most straight-forward (easiest) implementation (an entry in both tables containing values for all instructions in the fetch group) would in effect have a sum greater (no less than) than the number of instructions in a fetch group.

In regard to claim 35, Patt and Talcott further disclosed the limitations:

- *wherein said step of updating the selector table comprises the substeps of:*

- *determining if at least one of the first set of branch prediction bits correctly predicts the corresponding branch resolution outcome* (Patt: page 252, section 2)*;*
- *updating the corresponding entry in the selector table to a first logic value when the at least one of the first set of prediction bits correctly represents the branch resolution outcome* (Patt: page 252, section 2)*;*
- *determining if at least one of the second set of branch prediction bits correctly predicts the branch resolution outcome* (Patt: page 252, section 2)*; and*
- *updating the corresponding entry in the selector table to a second logical value when the at least one of the second set of branch prediction bits correctly represents the branch resolution outcome* (Patt: page 252, section 2).

In regard to claim 36, Patt and Talcott further disclosed the limitations:

- *determining if at least one bit of both the first and second sets of branch history bits correctly predict the branch resolution outcome* (Patt: page 252, section 2)*;*
- *maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome* (Patt: page 252, section 2)*;*

- *determining if at least one bit of both the first and second sets of branch prediction bits incorrectly predict the branch resolution outcome* (Patt: page 252, section 2)*; and*
- *maintaining the current value of corresponding bits in the corresponding selector table entry when the at least one bit of both the first and second sets of branch history bits incorrectly predict the branch history outcome* (Patt: page 252, section 2).

In regard to claim 37, Patt andTalcott further disclosed the limitations:

- *determining whether at least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome* (Patt: page 252, section 2)*;*
- *maintaining the current value of corresponding bits in the corresponding selector table entry when at the least one bit of both the first and second sets of branch prediction bits correctly predict the branch resolution outcome* (Patt: page 252, section 2)

Patt and Talcott did not explicitly state the limitation *updating the current selector table entry to a logic value associated with the fetch-based branch history table when neither of corresponding bits of the first and second sets of branch prediction bits correctly predicts the branch resolution outcome.* However, Patt did demonstrate that it was known at the time of invention that two-level branch prediction is the highest performance of the single predictors (page 253, first paragraph under bulleted items). It

would have been obvious to one of ordinary skill in the art at the time of invention to implement the Patt and Talcott selector table of single branch predictors with recording the fetch-based (or two level) table as the default choice when neither choice is correct as suggested by Patt's own teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to gradually adjust the predictor to the more likely correct future choice, especially if there is no evidence not to make such an adjustment (i.e. neither predictor proving accurate).

In regard to claim 38, Patt and Talcott further disclosed the limitation *wherein said step of accessing the fetch-based branch history table comprises the substep of generating an address from at least some bits of a branching instruction and bits retrieved from a history register* (Patt: page 253, fourth bulleted item).

In regard to claim 39, Patt and Talcott further disclosed the limitation *wherein the history register comprises a shift register* (Patt: page 253, fourth bulleted item; page 255, Figure 2 and sections 4 and 4.1).

4. Claims 23, 26-27 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patt et al., "Alternative Implementations of Hybrid Branch Predictors" in view of Talcott et al. (USPN 6,289,441).

In regard to claim 23, Patt and Talcott did not explicitly state the limitation *wherein said history register comprises a shift register and said branch prediction circuitry further comprises circuitry for updating said shift register by shifting in a preselected prediction value for each fetch group*. McFarling demonstrated that it was known at the time of invention to implement a hybrid branch prediction system with a *shifting* history register (page 6, section 5, first paragraph; pages 11-12, section 7). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the hybrid branch system using fetch groups of Patt and Talcott with a shift register for the history register as found in McFarling's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to make use of existing (and thus well understood) technology when implementing hybrid branch predictors.

In regard to claim 26, Patt and Talcott further disclosed the limitation *wherein said circuitry for updating said selector table is further operable to*

- *maintain a value in a selected entry in said selector table when corresponding values from said bimodal and fetch-based branch history tables both correctly represent a corresponding branch resolution* (Patt: page 252, section 2, first paragraph), *and*
- *wherein said circuitry for updating said selector table is further operable to maintain a value in a selected entry in said selector table when neither values from said bimodal and fetch-based branch history tables correctly represent a corresponding branch resolution* (Patt: page 252, section 2, first paragraph).

In regard to claim 27, Patt and Talcott did not explicitly state the limitation *wherein said circuitry for updating said selector table is further operable to set a value in a selected entry in said selector table to a value associated with said fetch-based table when corresponding values from said bimodal and fetch based branch history tables both do not correctly predict a corresponding branch resolution outcome*. However, Patt did demonstrate that it was known at the time of invention that two-level branch prediction is the highest performance of the single predictors (page 253, first paragraph under bulleted items). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the Patt and Talcott selector table of single branch predictors with recording the fetch-based (or two level) table as the default choice when neither choice is correct as suggested by Patt's own teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to gradually adjust the predictor to the more likely correct future choice, especially if there is no evidence not to make such an adjustment (i.e. neither predictor proving accurate).

In regard to claim 40, Patt and Talcott did not explicitly state the limitation *wherein said method further comprises the steps of updating the shift register by shifting in a prediction bit for each fetch group*. McFarling demonstrated that it was known at the time of invention to implement a hybrid branch prediction system with a *shifting* history register (page 6, section 5, first paragraph; pages 11-12, section 7). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the hybrid

branch system using fetch groups of Patt and Talcott with a shift register for the history register as found in McFarling's teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to make use of existing (and thus well understood) technology when implementing hybrid branch predictors.

Response to Arguments

5. Applicant's arguments with respect to claims 10 and 21-40 have been considered but are moot in view of the new ground(s) of rejection, which takes into account Applicant's issues of concern.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
October 30, 2003

TODD INGBERG
PRIMARY EXAMINER